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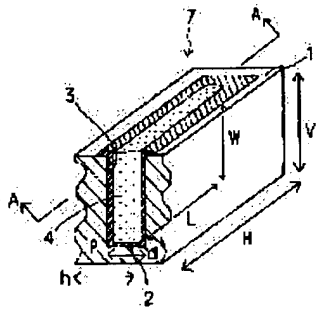
(54) RESISTANCE ELEMENTS AND SEMICONDUCTOR DEVICE IN WHICH SAID ELEMENTS ARE INTEGRATED

(57)Abstract:
PURPOSE: To provide a semiconductor device which restrains the influence upon the characteristics change of a semiconductor device to a minimum and improves the level of integration by facilitating reduction of the layout area of resistance elements with irregularity of resistance value kept restrained 4 to be small.
CONSTITUTION: A resistance element 7 is constituted by burying a resistor 4 composed of polycrystalline semiconductor having a desired resistance value, in a vertical trench 2 of a substrate 1 composed of a semiconductor substrate, interposing an insulating film 3. The resistor 4 has a resistance width W in the vertical direction V of the substrate 1, and a resistance length L in the horizontal direction H of the substrate 1, and is doped with impurities. By setting the resistance width W large in the vertical direction V, a desired resistance value can be obtained while the resistance length L in the horizontal direction H is small. Thereby the layout area of the resistance element 7 is easily reduced. Since a desired resistance value is obtained by adjusting the dosage of impurities, irregularity of the resistance value can be restrained in a small range.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention is applied to the resistance element accumulated as a 1 constituent child of a semiconductor device by the same semiconductor substrate as an active element about a resistance element, and relates to effective technology.
[0002]
[Description of the Prior Art] The resistance element which operates as a passive element in addition to the transistor to which semiconductor devices, such as IC and LSI, operate as an active element is accumulated by the same semiconductor substrate. This resistance element is simultaneously manufactured by the same semiconductor substrate using some processes of the manufacturing process in the case of manufacturing a transistor to a semiconductor substrate. For example, a resistance element is manufactured by the same semiconductor substrate as a transistor using a part of diffusion process which is a manufacturing process of a transistor.
[0003] Manufacture of such a resistance element is indicated by the edition [25 / per day / 1st edition] issue, and P102-P103 in Ohm-Sha Ltd. issue "guide to semiconductor integrated circuit" May, Showa 42. In this reference, the resistance manufactured by diffusion is simultaneous with diffusion of the emitter layer of a transistor, or being carried out simultaneously with diffusion of a base layer is indicated. Thus, both the resistance of the resistance element manufactured is determined depending on the value of the resistance length L and the resistance width of face W which are set as the front face and horizontal direction of a semiconductor substrate. That is, the required resistance depending on each value is obtained by setting the resistance length L and the resistance width of face W as the horizontal direction of a semiconductor substrate.
[0004]
[Problem(s) to be Solved by the Invention] Since the resistance length L and the resistance width of face W must be set as the horizontal direction of a semiconductor substrate according to this resistance for obtaining desired resistance when manufacturing the aforementioned resistance element to a semiconductor substrate, depending on resistance, it is not avoided that the resistance length L and a value with the horizontal resistance width of face W become large. Therefore, the problem that the layout area occupied to a semiconductor substrate becomes large arises.
[0005] Moreover, when accumulating this resistance element on the same semiconductor substrate as an active element like a transistor and manufacturing a semiconductor device, it becomes indispensable to reduce not only the layout area of a transistor but the layout area of a resistance element for aiming at improvement in the degree of integration of a semiconductor device. Here, although the layout area of a transistor is comparatively easy to reduce by improvement in the latest process processing technology, about a resistance element, reduction of layout area becomes difficult for the above reasons. Moreover, if it is going to reduce the layout area of a resistance element by force, since resistance tends to vary greatly in manufacture from the first, a resistance element will come to affect property change of a semiconductor device with reduction.
[0006] The purpose of this invention has reduction of layout area in offering an easy resistance element.
[0007] Other purposes of this invention are for reduction of layout area to offer an easy resistance element, suppressing dispersion in resistance small.
[0008] The purpose of others of this invention is by making reduction of the layout area of a resistance element easy, suppressing dispersion in resistance small to suppress to minimum the influence affect property change of a semiconductor device, and offer the semiconductor device which aims at improvement in a degree of integration.
[0009] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.
[0010]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0011] (1) A perpendicular slot is formed alternatively [the resistance element of this invention] to a substrate, and the insulator layer is formed in the internal surface of the perpendicular slot of this substrate. While an insulator layer is placed between perpendicular Mizouchi of a substrate and having resistance width of face to the perpendicular direction of a

substrate, the resistor which has resistance length is laid under the horizontal direction of a substrate.
[0012] (2) A perpendicular slot is formed alternatively [other resistance elements of this invention] to a semiconductor substrate, and the insulator layer is formed in the internal surface of the perpendicular slot of this semiconductor substrate. The resistor which consists of a polycrystal semiconductor formed so that an insulator layer is placed between perpendicular Mizouchi of a semiconductor substrate, it had resistance length to the horizontal direction of a semiconductor substrate while having resistance width of face to the perpendicular direction of a semiconductor substrate, and an impurity might be doped and it might have desired resistance is laid underground.
[0013] (3) As for the semiconductor device of this invention, the active element is accumulated on the position of a request of a semiconductor substrate. Moreover, the perpendicular slot alternatively formed in other positions of a semiconductor substrate at this semiconductor substrate, The insulator layer formed in the internal surface of this perpendicular slot and aforementioned perpendicular Mizouchi intervene and lay an insulator layer underground. The resistance element which consisted of resistors which consist of a polycrystal semiconductor formed so that it had resistance length to the horizontal direction of the aforementioned semiconductor substrate while having resistance width of face to the perpendicular direction of the aforementioned semiconductor substrate, and an impurity might be doped and it might have desired resistance is accumulated.
[0014]
[Function] According to the means of (1) mentioned above, since the resistor which has resistance length is laid underground and constituted by the horizontal direction of a substrate while an insulator layer is placed between perpendicular Mizouchi of a substrate by the resistance element of this invention and having resistance width of face to the perpendicular direction of a substrate, reduction of the layout area of a resistance element becomes easy.
[0015] Reduction of the layout area of a resistance element becomes easy, suppressing dispersion in resistance small, since the resistor which consists of a polycrystal semiconductor which has resistance length to the horizontal direction of a semiconductor substrate while an insulator layer is placed between perpendicular Mizouchi of a semiconductor substrate by the resistance element of this invention and having resistance width of face to the perpendicular direction of a semiconductor substrate, and an impurity is doped and has desired resistance was laid underground and constituted according to the means of (2) mentioned above.
[0016] According to the means of (3) mentioned above, the semiconductor device of this invention An active element is accumulated on the position of a request of the same semiconductor substrate. in other positions While an insulator layer is placed between perpendicular Mizouchi of the aforementioned semiconductor substrate and having resistance width of face to the perpendicular direction of a semiconductor substrate, it has resistance length to the horizontal direction of a semiconductor substrate. Since the resistance element which the resistor which consists of a polycrystal semiconductor which an impurity is doped and has desired resistance laid underground and consisted of is accumulated Reduction of the layout area of a resistance element can become easy, suppressing dispersion in resistance small, the influence affect property change of a semiconductor device can be suppressed to minimum, and improvement in a degree of integration can be aimed at.
[0017]
[Example] With reference to a drawing, the example of this invention is explained below.
[0018] (Example 1) Drawing 1 is the perspective diagram showing the resistance element by the example 1 of this invention, and drawing 2 is the A-A cross section of drawing 1 . 1 is the substrate which consists of a silicon-single-crystal substrate of for example, P conductivity type, and the perpendicular slot 2 is alternatively formed in this substrate 1. This perpendicular slot 2 has the size L of other horizontally H it intersects perpendicularly with the horizontal direction h (equivalent to the below-mentioned resistance length L) while it has the so-called trench structure and has the size W (equivalent to the below-mentioned resistance width of face W) of the larger perpendicular direction V than the size d of the horizontal direction h of a substrate 1 (equivalent to the below-mentioned thickness d). In addition, horizontally [other / H] it intersects perpendicularly with a horizontal direction h and this shows the relative relation, and if they are horizontal to the front face of a substrate 1, they can choose all as any sense. Such a perpendicular slot 2 is formed using processing technology, such as anisotropic etching processing. For example, this perpendicular slot 2 is formed of the anisotropic etching by reactive ion etching (Reactive Ion Etching) so that it may mention later.
[0019] 3 is the insulator layer which consists for example, of 2 silicon oxides (SiO_2), and is formed in the internal surface of the perpendicular slot 2 using vapor-growth technology, such as CVD. 4 is the resistor which consists for example, of polycrystal silicon, it is formed using vapor-growth technology, such as CVD, and an insulator layer 3 is intervened and laid underground in the perpendicular slot 2. An impurity, for example, boron, phosphorus, arsenic, antimony, etc. are doped by the resistor 4 which consists of this polycrystal silicon using an ion implantation method etc., and it is formed so that it may have desired resistance. Here, it is formed so that it may have the resistance length L to the horizontal direction H of a substrate 1, and the resistor 4 which consists of this polycrystal silicon is formed so that it may have thickness d to a horizontal direction h further while it has the resistance width of face W to the perpendicular direction V of a substrate 1.
[0020] By this, this resistor 4 will have the resistance of the request determined by (resistance width-of-face Wx resistance length Lx thickness d). Here, since the value of =(resistance width-of-face Wx thickness d) A shows the cross section of a resistor 4 and resistance is shown by (the cross-section Ax resistance length L), when obtaining fixed resistance, the resistance length L can do small by setting up the resistance width of face W greatly. This means that layout area of the resistor 4 occupied to a substrate 1 is made small.

[0021] As shown in drawing 2 , it is constituted as a resistance element 7 by the resistor 4 which consists of polycrystal silicon formed so that it might have desired resistance by pulling out the electrode 5 of a couple which consists of aluminum on the insulator layer 3 of a substrate 1. The front face of a resistor 4 is protected by the insulator layers 6, such as 2 silicon oxides. Front faces other than the position in which the resistance element 7 of a substrate 1 was formed are protected by an insulator layer 3 or other insulator layers.

[0022] Next, with reference to drawing 3 or drawing 7 , the manufacture method of the resistance element of an example 1 is explained in order of a process. As shown in drawing 3 , the substrate 1 which consists of a silicon-single-crystal substrate of P conductivity type is prepared first, and a photoresist 8 is applied in addition to the front face which should form the perpendicular slot of this substrate 1. next, it is shown in drawing 4 -- as -- a substrate 1 -- receiving -- for example, SF6 CCl4 mixed gas is supplied and it is based on RIE -- different -- modality -- the perpendicular slot 2 which has a size d to a size W and a horizontal direction h, and has a size L to a perpendicular direction V alternatively and as mentioned above at other horizontal directions H is formed in substrate 1 front face on which it etches and the photoresist 8 is not applied Then, it is as opposed to / a substrate 1 / after removing a photoresist 8, as it is shown in drawing 5] SiH4. O2 Mixed gas is supplied, the vapor growth by CVD is performed, and the insulator layer 3 which consists of 2 silicon oxides is formed in substrate 1 front face containing the internal surface of the perpendicular slot 2.

[0023] Next, it is [as opposed to / a substrate 1 / as shown in drawing 6] SiCl4. H2 Mixed gas is supplied, the vapor growth by CVD is performed, and the resistor 4 which intervenes an insulator layer 3 in the perpendicular slot 2, and consists of polycrystal silicon is laid underground. Then, as shown in drawing 7 , after driving for example, + boron ion into the resistor 4 which consists of this polycrystal silicon by the ion implantation method, by performing heat treatment, boron is doped and a resistor 4 is controlled to desired resistance. On the occasion of placing of boron, boron can be doped by carrying out the mask of the garbage by the photoresist 8 only to the resistor 4 which consists of polycrystal silicon.

[0024] Next, as shown in drawing 2 , it forms so that the electrode 5 of a couple may be pulled out on the insulator layer 3 of a substrate 1 from the both ends of a resistor 4 which consist of polycrystal silicon. After this adheres aluminum to the whole surface by CVD etc., it performs photo etching and performs it by removing a garbage. Then, the above CVD etc. is used for the front face of a resistor 4, and the insulator layer 6 which consists of 2 silicon oxides is formed in it. The insulator layer 3 of the front face of a substrate 1 may use the 2 silicon oxides which could use the 2 silicon oxides formed at the time of the process of drawing 5 as they were, or grew thermally from the substrate 1. The resistance element 7 of an example 1 is manufactured according to each above process.

[0025] According to such an example 1, the following effects are acquired.

[0026] (1) Since the resistor 4 which has the resistance length L is laid underground and constituted by the horizontal direction H of a substrate 1 while a resistance element 7 intervenes an insulator layer 3 in the perpendicular slot 2 of a substrate 1 and having the resistance width of face W to the perpendicular direction V of a substrate 1, the resistance length L of a horizontal direction H makes it small by taking the large resistance width of face W to a perpendicular direction V and desired resistance is obtained, reduction of the layout area of a resistance element 7 becomes easy.

[0027] (2) A resistance element 7 has the resistance length L to the horizontal direction H of a substrate 1 while it intervenes an insulator layer 3 in the perpendicular slot 2 of the substrate 1 which consists of a semiconductor substrate and has the resistance width of face W to the perpendicular direction V of a substrate 1. Since the resistor 4 which consists of a polycrystal semiconductor which an impurity is doped and has desired resistance is laid underground and constituted and desired resistance is obtained with the amount of dopes of an impurity, reduction of the layout area of ********** 7 which suppressed dispersion in resistance small becomes easy.

[0028] (Example 2) Drawing 9 is the cross section showing the semiconductor device by the example 2, the structure which accumulated the resistance element 7 linked to the transistor 10 which consists of an NPN transistor, and the emitter region of this transistor 10 of circuitry as shown in drawing 8 on the same semiconductor substrate is shown, and drawing 10 is the plan showing the circuit pattern of drawing 9 . The transistor 10 which consists of a NPN type transistor which operates as an active element which consists of the collector field 12 of N conductivity type, a base region 13 of P conductivity type alternatively formed in this collector field 12, and an emitter region 14 of N conductivity type alternatively formed in this base region 13 is accumulated on the island 11 insulated in the isolation field 9 which is the request position of the substrate 1 which consists of a silicon-single-crystal substrate of a semiconductor device 16, for example, P conductivity type. The collector field 12, a base region 13, and an emitter region 14 are formed using a diffusion method, an ion implantation method, etc. The front face of a transistor 10 is protected by the insulator layer 15 which grew at the time of formation of each fields 12, 13, and 14 and which consists of 2 silicon oxides, for example. In addition, the conductivity type of each fields 12, 13, and 14 can show an example, and can choose a reverse conductivity type.

[0029] On the other hand, in other positions of the substrate 1 of a semiconductor device 16 The perpendicular slot 2 which has a size d to a size W and a horizontal direction h, and has a size L to other horizontal directions H perpendicularly [V] it was alternatively formed in the substrate 1, The insulator layer 3 which was formed in the internal surface of this perpendicular slot 2 and which consists of diacid-ized silicon, for example, While intervening and laying an insulator layer 3 underground in the perpendicular slot 2 and having the resistance width of face W to the perpendicular direction V of a substrate 1, it has the resistance length L to the horizontal direction H of a substrate 1. It consists of resistors 4 which consist of a polycrystal semiconductor formed so that an impurity might be doped and it might have desired resistance, and the resistance element 7 which has the electrode 5 of a couple which was pulled out from this resistor 4, and which consists of

aluminum, for example is accumulated. This resistance element 7 is manufactured by the aforementioned manufacture method.

[0030] It connects with an emitter region 14 through contact hole 14E which the insulator layer 15 top was extended and was formed in the insulator layer 15 on the emitter region 14 of a transistor 10, and one side of the electrode 5 of the couple pulled out from the resistance element 7 works as emitter electrode 14e. Moreover, base-electrode 13b is pulled out through contact hole 13B formed in the insulator layer 15 on the **-SU field 13, and collector-electrode 12c is further pulled out through contact hole 12C formed in the insulator layer 15 on a collector 12.

[0031] According to such an example 2, the following effects are acquired.

[0032] Reduction of the layout area of a resistance element 7 can become easy, suppressing dispersion in resistance small, since the transistor 10 which operates as an active element was accumulated on the position of a request of the same substrate 1 and the resistance element 7 of the structure shown in the aforementioned example 1 was accumulated on other positions, and a semiconductor device 16 can suppress to minimum the influence affect property change of a semiconductor device 16, and can aim at improvement in a degree of integration.

[0033] As mentioned above, although invention made by this invention person was concretely explained based on the aforementioned example, this invention of the ability to change variously in the range which is not limited to the aforementioned example and does not deviate from the summary is natural.

[0034] For example, although the example which uses a silicon-single-crystal substrate as a substrate 1 explained in each aforementioned example, this substrate 1 can use the single crystal substrate which consists not only of silicon but of other semiconductor materials. Moreover, you may make it this substrate 1 use what consists of an insulating material not only like a semiconductor material but ceramics. Thus, when the substrate 1 which consists of an insulating material is used, the transistor which operates as an active element which constitutes a semiconductor device is mounted in the front face of this substrate 1 in the form of a chip.

[0035] Moreover, although the example which uses diacid-ized silicon as an insulator layer 3 explained in each aforementioned example, this insulator layer 3 can use not only this but other insulating materials. For example, other insulating materials, such as a silicon nitride (Si 3N4) and an aluminum oxide (aluminum 2O3), can be used, and these insulating materials can be formed using vapor-growth technology, such as CVD, like the case of diacid-ized silicon. Furthermore, this insulator layer 3 may be formed from two or more layers which consist not only of a monostromatic but of the same material or different material.

[0036] Moreover, although the example which uses polycrystal silicon as a resistor 4 explained in the aforementioned example, this resistor 4 can use not only silicon but other semiconductor materials. Furthermore, the impurity doped to this resistor 4 can use the impurity of others, such as phosphorus, arsenic, and antimony, without restricting to a specific impurity like boron. You may make it use electrical resistance materials other than a semiconductor material as this resistor 4 further again.

[0037] Although the above explanation explained the case where invention mainly made by this invention person was applied to the formation technology of the resistance element which is a field of the invention used as the background, it is not limited to it. this invention is applicable to the thing of the conditions which form a perpendicular slot in a substrate at least, lay a resistor under this perpendicular Mizouchi and form an element.

[0038]

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.

[0039] Reduction of the layout area of a resistance element becomes easy.

[0040] Reduction of the layout area of a resistance element becomes easy, suppressing dispersion in resistance small.

[0041] Reduction of the layout area of a resistance element can become easy, suppressing dispersion in resistance small, the influence affect property change of a semiconductor device can be suppressed to minimum, and improvement in a degree of integration can be aimed at.

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1] The resistance element characterized by consisting of a substrate in which the perpendicular slot was formed alternatively, an insulator layer formed in the internal surface of the perpendicular slot of this substrate, and a resistor which has resistance length to the horizontal direction of the aforementioned substrate while aforementioned perpendicular Mizouchi intervenes and lays an insulator layer underground and having resistance width of face to the perpendicular direction of the aforementioned substrate.
[Claim 2] It is the resistance element according to claim 1 to which the aforementioned resistor is characterized by the bird clapper from a polycrystal semiconductor while the aforementioned substrate consists of a semiconductor substrate.
[Claim 3] The resistance element characterized by consisting of resistors which consist of a polycrystal semiconductor formed so that it both had resistance length to the horizontal direction of the aforementioned semiconductor substrate as it is characterized by providing the following, and an impurity might be doped and it might have desired resistance. The semiconductor substrate in which the perpendicular slot was formed alternatively. The insulator layer formed in the internal surface of the perpendicular slot of this substrate. Aforementioned perpendicular Mizouchi intervenes and lays an insulator layer underground, and it is resistance width of face to the perpendicular direction of the aforementioned semiconductor substrate.
[Claim 4] The semiconductor device characterized by providing the following. The perpendicular slot which was accumulated on other positions of the active element accumulated on the position of a request of a semiconductor substrate, and the aforementioned semiconductor substrate, and was alternatively formed in the aforementioned semiconductor substrate. The insulator layer formed in the internal surface of this perpendicular slot. The resistance element which consisted of resistors which consist of a polycrystal semiconductor formed so that aforementioned perpendicular Mizouchi intervenes and lays an insulator layer underground, it had resistance length to the horizontal direction of the aforementioned semiconductor substrate while having resistance width of face to the perpendicular direction of the aforementioned semiconductor substrate, and an impurity might be doped and it might have desired resistance.

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TECHNICAL FIELD

[Industrial Application] Especially this invention is applied to the resistance element accumulated as a 1 constituent child of a semiconductor device by the same semiconductor substrate as an active element about a resistance element, and relates to effective technology.

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MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0011] (1) A perpendicular slot is formed alternatively [the resistance element of this invention] to a substrate, and the insulator layer is formed in the internal surface of the perpendicular slot of this substrate. While an insulator layer is placed between perpendicular Mizouchi of a substrate and having resistance width of face to the perpendicular direction of a substrate, the resistor which has resistance length is laid under the horizontal direction of a substrate.
[0012] (2) A perpendicular slot is formed alternatively [other resistance elements of this invention] to a semiconductor substrate, and the insulator layer is formed in the internal surface of the perpendicular slot of this semiconductor substrate. The resistor which consists of a polycrystal semiconductor formed so that an insulator layer is placed between perpendicular Mizouchi of a semiconductor substrate, it had resistance length to the horizontal direction of a semiconductor substrate while having resistance width of face to the perpendicular direction of a semiconductor substrate, and an impurity might be doped and it might have desired resistance is laid underground.
[0013] (3) As for the semiconductor device of this invention, the active element is accumulated on the position of a request of a semiconductor substrate. Moreover, the perpendicular slot alternatively formed in other positions of a semiconductor substrate at this semiconductor substrate, The insulator layer formed in the internal surface of this perpendicular slot and aforementioned perpendicular Mizouchi intervene and lay an insulator layer underground. The resistance element which consisted of resistors which consist of a polycrystal semiconductor formed so that it had resistance length to the horizontal direction of the aforementioned semiconductor substrate while having resistance width of face to the perpendicular direction of the aforementioned semiconductor substrate, and an impurity might be doped and it might have desired resistance is accumulated.

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OPERATION

[Function] According to the means of (1) mentioned above, since the resistor which has resistance length is laid underground and constituted by the horizontal direction of a substrate while an insulator layer is placed between perpendicular Mizouchi of a substrate by the resistance element of this invention and having resistance width of face to the perpendicular direction of a substrate, reduction of the layout area of a resistance element becomes easy.
[0015] Reduction of the layout area of a resistance element becomes easy, suppressing dispersion in resistance small, since the resistor which consists of a polycrystal semiconductor which has resistance length to the horizontal direction of a semiconductor substrate while an insulator layer is placed between perpendicular Mizouchi of a semiconductor substrate by the resistance element of this invention and having resistance width of face to the perpendicular direction of a semiconductor substrate, and an impurity is doped and has desired resistance was laid underground and constituted according to the means of (2) mentioned above.
[0016] According to the means of (3) mentioned above, it is the semiconductor device of this invention. An active element is accumulated on the position of a request of the same semiconductor substrate. in other positions While an insulator layer is placed between perpendicular Mizouchi of the aforementioned semiconductor substrate and having resistance width of face to the perpendicular direction of a semiconductor substrate, it has resistance length to the horizontal direction of a semiconductor substrate. Since the resistance element which the resistor which consists of a polycrystal semiconductor which an impurity is doped and has desired resistance laid underground and consisted of is accumulated Reduction of the layout area of a resistance element can become easy, suppressing dispersion in resistance small, the influence affect property change of a semiconductor device can be suppressed to minimum, and improvement in a degree of integration can be aimed at.

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EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0039] Reduction of the layout area of a resistance element becomes easy.
[0040] Reduction of the layout area of a resistance element becomes easy, suppressing dispersion in resistance small.
[0041] Reduction of the layout area of a resistance element can become easy, suppressing dispersion in resistance small, the influence affect property change of a semiconductor device can be suppressed to minimum, and improvement in a degree of integration can be aimed at.

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EXAMPLE

[Example] With reference to a drawing, the example of this invention is explained below.
[0018] (Example 1) Drawing 1 is the perspective diagram showing the resistance element by the example 1 of this invention, and drawing 2 is the A-A cross section of drawing 1 . 1 is the substrate which consists of a silicon-single-crystal substrate of for example, P conductivity type, and the perpendicular slot 2 is alternatively formed in this substrate 1. This perpendicular slot 2 has the size L of other horizontally H it intersects perpendicularly with the horizontal direction h (equivalent to the below-mentioned resistance length L) while it has the so-called trench structure and has the size W (equivalent to the below-mentioned resistance width of face W) of the larger perpendicular direction V than the size d of the horizontal direction h of a substrate 1 (equivalent to the below-mentioned thickness d). In addition, horizontally [other / H] it intersects perpendicularly with a horizontal direction h and this shows the relative relation, and if they are horizontal to the front face of a substrate 1, they can choose all as any sense. Such a perpendicular slot 2 is formed using processing technology, such as anisotropic etching processing. For example, this perpendicular slot 2 is formed of the anisotropic etching by reactive ion etching (Reactive Ion Etching) so that it may mention later.
[0019] 3 is the insulator layer which consists for example, of diacid-ized silicon (SiO2), and is formed in the internal surface of the perpendicular slot 2 using vapor-growth technology, such as CVD. 4 is the resistor which consists for example, of polycrystal silicon, it is formed using vapor-growth technology, such as CVD, and an insulator layer 3 is intervened and laid underground in the perpendicular slot 2. An impurity, for example, boron, phosphorus, arsenic, antimony, etc. are doped by the resistor 4 which consists of this polycrystal silicon using an ion implantation method etc., and it is formed so that it may have desired resistance. Here, it is formed so that it may have the resistance length L to the horizontal direction H of a substrate 1, and the resistor 4 which consists of this polycrystal silicon is formed so that it may have thickness d to a horizontal direction h further while it has the resistance width of face W to the perpendicular direction V of a substrate 1.
[0020] By this, this resistor 4 will have the resistance of the request determined by (resistance width-of-face Wx resistance length Lx thickness d). Here, since the value of =(resistance width-of-face Wx thickness d) A shows the cross section of a resistor 4 and resistance is shown by (the cross-section Ax resistance length L), when obtaining fixed resistance, the resistance length L can do small by setting up the resistance width of face W greatly. This means that layout area of the resistor 4 occupied to a substrate 1 is made small.
[0021] As shown in drawing 2 , it is constituted as a resistance element 7 by the resistor 4 which consists of polycrystal silicon formed so that it might have desired resistance by pulling out the electrode 5 of a couple which consists of aluminum on the insulator layer 3 of a substrate 1. The front face of a resistor 4 is protected by the insulator layers 6, such as diacid-ized silicon. Front faces other than the position in which the resistance element 7 of a substrate 1 was formed are protected by an insulator layer 3 or other insulator layers.
[0022] Next, with reference to drawing 3 or drawing 7 , the manufacture method of the resistance element of an example 1 is explained in order of a process. As shown in drawing 3 , the substrate 1 which consists of a silicon-single-crystal substrate of P conductivity type is prepared first, and a photoresist 8 is applied in addition to the front face which should form the perpendicular slot of this substrate 1. next, it is shown in drawing 4 -- as -- a substrate 1 -- receiving -- for example, SF6 CCl4 mixed gas is supplied and it is based on RIE -- different -- modality -- the perpendicular slot 2 which has a size d to a size W and a horizontal direction h, and has a size L to a perpendicular direction V alternatively and as mentioned above at other horizontal directions H is formed in substrate 1 front face on which it etches and the photoresist 8 is not applied Then, it is as opposed to / a substrate 1 / after removing a photoresist 8, as it is shown in drawing 5] SiH4. O2 Mixed gas is supplied, the vapor growth by CVD is performed, and the insulator layer 3 which consists of diacid-ized silicon is formed in substrate 1 front face containing the internal surface of the perpendicular slot 2.
[0023] Next, it is [as opposed to / a substrate 1 / as shown in drawing 6] SiCl4. H2 Mixed gas is supplied, the vapor growth by CVD is performed, and the resistor 4 which intervenes an insulator layer 3 in the perpendicular slot 2, and consists of polycrystal silicon is laid underground. Then, as shown in drawing 7 , after driving for example, + boron ion into the resistor 4 which consists of this polycrystal silicon by the ion implantation method, by performing heat treatment, boron is doped and a resistor 4 is controlled to desired resistance. On the occasion of placing of boron, boron can be doped by carrying out the mask of the garbage by the photoresist 8 only to the resistor 4 which consists of polycrystal silicon.
[0024] Next, as shown in drawing 2 , it forms so that the electrode 5 of a couple may be pulled out on the insulator layer 3 of a substrate 1 from the both ends of a resistor 4 which consist of polycrystal silicon. After this adheres aluminum to the whole

aforementioned example, this insulator layer 3 can use not only this but other insulating materials. For example, other insulating materials, such as a silicon nitride (Si 3N4) and an aluminum oxide (aluminum 2O3), can be used, and these insulating materials can be formed using vapor-growth technology, such as CVD, like the case of diacid-ized silicon. Furthermore, this insulator layer 3 may be formed from two or more layers which consist not only of a monostromatic but of the same material or different material.

[0036] Moreover, although the example which uses polycrystal silicon as a resistor 4 explained in the aforementioned example, this resistor 4 can use not only silicon but other semiconductor materials. Furthermore, the impurity doped to this resistor 4 can use the impurity of others, such as phosphorus, arsenic, and antimony, without restricting to a specific impurity like boron. You may make it use electrical resistance materials other than a semiconductor material as this resistor 4 further again.

[0037] Although the above explanation explained the case where invention mainly made by this invention person was applied to the formation technology of the resistance element which is a field of the invention used as the background, it is not limited to it. this invention is applicable to the thing of the conditions which form a perpendicular slot in a substrate at least, lay a resistor under this perpendicular Mizouchi and form an element.

[Translation done.]

surface by CVD etc., it performs photo etching and performs it by removing a garbage. Then, the above CVD etc. is used for the front face of a resistor 4, and the insulator layer 6 which consists of diacid-ized silicon is formed in it. The insulator layer 3 of the front face of a substrate 1 may use the diacid-ized silicon which could use the diacid-ized silicon formed at the time of the process of drawing 5 as it was, or grew thermally from the substrate 1. The resistance element 7 of an example 1 is manufactured according to each above process.

[0025] According to such an example 1, the following effects are acquired.

[0026] (1) Since the resistor 4 which has the resistance length L is laid underground and constituted by the horizontal direction H of a substrate 1 while a resistance element 7 intervenes an insulator layer 3 in the perpendicular slot 2 of a substrate 1 and having the resistance width of face W to the perpendicular direction V of a substrate 1, the resistance length L of a horizontal direction H makes it small by taking the large resistance width of face W to a perpendicular direction V and desired resistance is obtained, reduction of the layout area of a resistance element 7 becomes easy.

[0027] (2) A resistance element 7 has the resistance length L to the horizontal direction H of a substrate 1 while it intervenes an insulator layer 3 in the perpendicular slot 2 of the substrate 1 which consists of a semiconductor substrate and has the resistance width of face W to the perpendicular direction V of a substrate 1. Since the resistor 4 which consists of a polycrystal semiconductor which an impurity is doped and has desired resistance is laid underground and constituted and desired resistance is obtained with the amount of dopes of an impurity, reduction of the layout area of ********** 7 which suppressed dispersion in resistance small becomes easy.

[0028] (Example 2) Drawing 9 is the cross section showing the semiconductor device by the example 2, the structure which accumulated the resistance element 7 linked to the transistor 10 which consists of an NPN transistor, and the emitter region of this transistor 10 of circuitry as shown in drawing 8 on the same semiconductor substrate is shown, and drawing 10 is the plan showing the circuit pattern of drawing 9 . The transistor 10 which consists of a NPN type transistor which operates as an active element which consists of the collector field 12 of N conductivity type, a base region 13 of P conductivity type alternatively formed in this collector field 12, and an emitter region 14 of N conductivity type alternatively formed in this base region 13 is accumulated on the island 11 insulated in the isolation field 9 which is the request position of the substrate 1 which consists of a silicon-single-crystal substrate of a semiconductor device 16, for example, P conductivity type. The collector field 12, a base region 13, and an emitter region 14 are formed using a diffusion method, an ion implantation method, etc. The front face of a transistor 10 is protected by the insulator layer 15 which grew at the time of formation of each fields 12, 13, and 14 and which consists of diacid-ized silicon, for example. In addition, the conductivity type of each fields 12, 13, and 14 can show an example, and can choose a reverse conductivity type.

[0029] On the other hand, in other positions of the substrate 1 of a semiconductor device 16 The perpendicular slot 2 which has a size d to a size W and a horizontal direction h, and has a size L to other horizontal directions H perpendicularly [V] it was alternatively formed in the substrate 1, The insulator layer 3 which was formed in the internal surface of this perpendicular slot 2 and which consists of diacid-ized silicon, for example, While intervening and laying an insulator layer 3 underground in the perpendicular slot 2 and having the resistance width of face W to the perpendicular direction V of a substrate 1, it has the resistance length L to the horizontal direction H of a substrate 1. It consists of resistors 4 which consist of a polycrystal semiconductor formed so that an impurity might be doped and it might have desired resistance, and the resistance element 7 which has the electrode 5 of a couple which was pulled out from this resistor 4, and which consists of aluminum, for example is accumulated. This resistance element 7 is manufactured by the aforementioned manufacture method.

[0030] It connects with an emitter region 14 through contact hole 14E which the insulator layer 15 top was extended and was formed in the insulator layer 15 on the emitter region 14 of a transistor 10, and one side of the electrode 5 of the couple pulled out from the resistance element 7 works as emitter electrode 14e. Moreover, base-electrode 13b is pulled out through contact hole 13B formed in the insulator layer 15 on the **-SU field 13, and collector-electrode 12c is further pulled out through contact hole 12C formed in the insulator layer 15 on a collector 12.

[0031] According to such an example 2, the following effects are acquired.

[0032] Reduction of the layout area of a resistance element 7 can become easy, suppressing dispersion in resistance small, since the transistor 10 which operates as an active element was accumulated on the position of a request of the same substrate 1 and the resistance element 7 of the structure shown in the aforementioned example 1 was accumulated on other positions, and a semiconductor device 16 can suppress to minimum the influence affect property change of a semiconductor device 16, and can aim at improvement in a degree of integration.

[0033] As mentioned above, although invention made by this invention person was concretely explained based on the aforementioned example, this invention of the ability to change variously in the range which is not limited to the aforementioned example and does not deviate from the summary is natural.

[0034] For example, although the example which uses a silicon-single-crystal substrate as a substrate 1 explained in each aforementioned example, this substrate 1 can use the single crystal substrate which consists not only of silicon but of other semiconductor materials. Moreover, you may make it this substrate 1 use what consists of an insulating material not only like a semiconductor material but ceramics. Thus, when the substrate 1 which consists of an insulating material is used, the transistor which operates as an active element which constitutes a semiconductor device is mounted in the front face of this substrate 1 in the form of a chip.

[0035] Moreover, although the example which uses diacid-ized silicon as an insulator layer 3 explained in each

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the perspective diagram showing the resistance element by the example 1 of this invention.
[Drawing 2] It is the A-A cross section of drawing 1 .
[Drawing 3] It is the cross section showing one process of the manufacture method of the resistance element by the example 1 of this invention.
[Drawing 4] It is the cross section showing other processes of the manufacture method of the resistance element by the example 1 of this invention.
[Drawing 5] It is the cross section showing the process of others of the manufacture method of the resistance element by the example 1 of this invention.
[Drawing 6] It is the cross section showing the process of others of the manufacture method of the resistance element by the example 1 of this invention.
[Drawing 7] It is the cross section showing the process of others of the manufacture method of the resistance element by the example 1 of this invention.
[Drawing 8] It is the circuitry view of the semiconductor device by the example 2 of this invention.
[Drawing 9] It is the cross section showing the semiconductor device by the example 2 of this invention.
[Drawing 10] It is the plan showing the semiconductor device by the example 2 of this invention.
[Description of Notations]
1 [-- An insulator layer, 4 / -- A resistor, 5 / -- The electrode of a couple,] -- A substrate, 2 -- A perpendicular slot, 3 6 [-- A photoresist, 9 / -- Isolation field,] -- An insulator layer, 7 -- A resistance element, 8 10 [-- Collector field,] -- A transistor (active element), 11 -- An island, 12 12E [-- A base region, 13B / -- A base contact hole, 13b / -- A base electrode, 14 / -- An emitter region, 14E / -- An emitter contact hole, 14e / -- An emitter electrode, 15 / -- An insulator layer, 16 / -- Semiconductor device.] -- A collector contact hole, 12e -- A collector electrode, 13

[Translation done.]

* NOTICES *

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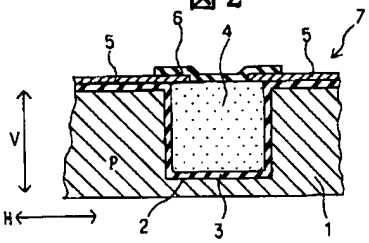
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

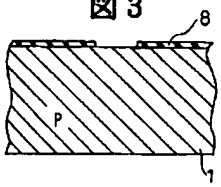
[Drawing 2]

図 2



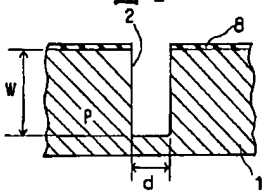
[Drawing 3]

図 3



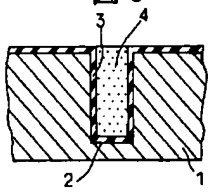
[Drawing 4]

図 4



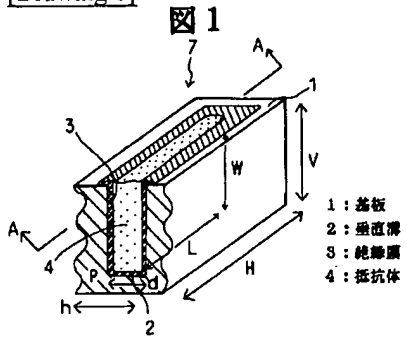
[Drawing 6]

図 6



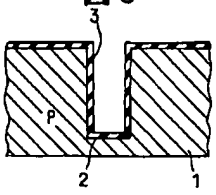
[Drawing 1]

図 1



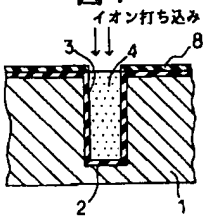
[Drawing 5]

図5



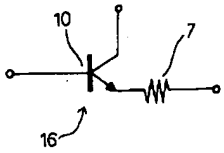
[Drawing 7]

図7



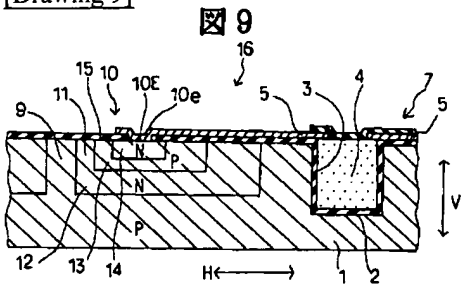
[Drawing 8]

図8



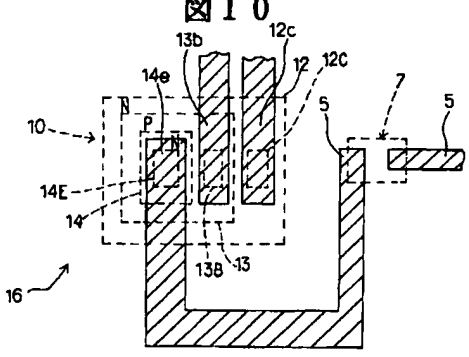
[Drawing 9]

図9



[Drawing 10]

図10



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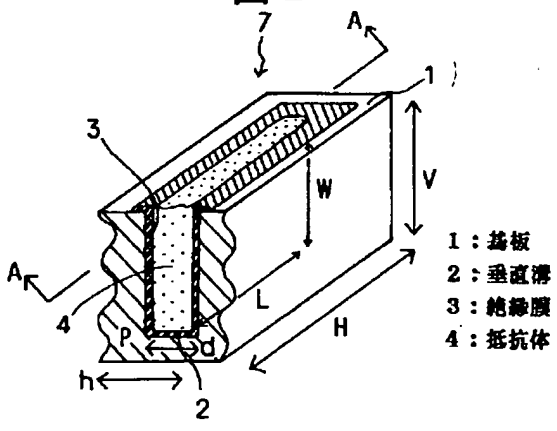
(54)【発明の名称】　抵抗素子及びこれが集積された半導体装置

(57)【要約】

【目的】　レイアウト面積の縮小が容易な抵抗素子及び、抵抗値のばらつきを小さく抑えたまま抵抗素子のレイアウト面積の縮小を容易にすることにより、半導体装置の特性変動に及ぼす影響を最低限に抑えて、集積度の向上を図る半導体装置を提供する。

【構成】　半導体基板からなる基板１の垂直溝２内に、絶縁膜３を介在して基板１の垂直方向Ｖに抵抗幅Ｗを有すると共に基板１の水平方向Ｈに抵抗長Ｌを有し、不純物がドープされて所望の抵抗値を有する多結晶半導体からなる抵抗体４を埋設して、抵抗素子７を構成する。抵抗幅Ｗを垂直方向Ｖに大きくとることにより水平方向Ｈの抵抗長Ｌは小さくして所望の抵抗値が得られるため、抵抗素子７のレイアウト面積の縮小が容易になる。また、不純物のドープ量により所望の対抗値が得られるため、抵抗値のばらつきを小さく抑えることができる。

図１



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【特許請求の範囲】

【請求項1】　選択的に垂直溝が形成された基板と、この基板の垂直溝の内壁面に形成された絶縁膜と、前記垂直溝内に絶縁膜を介在して埋設され、前記基板の垂直方向に抵抗幅を有すると共に前記基板の水平方向に抵抗長を有する抵抗体とから構成されたことを特徴とする抵抗素子。

【請求項2】　前記基板は半導体基板からなると共に、前記抵抗体は多結晶半導体からなることを特徴とする請求項1記載の抵抗素子。

【請求項3】　選択的に垂直溝が形成された半導体基板と、この基板の垂直溝の内壁面に形成された絶縁膜と、前記垂直溝内に絶縁膜を介在して埋設され、前記半導体基板の垂直方向に抵抗幅を有すると共に前記半導体基板の水平方向に抵抗長を有し、不純物がドープされて所望の抵抗値を有するように形成された多結晶半導体からなる抵抗体とから構成されたことを特徴とする抵抗素子。

【請求項4】　半導体基板の所望の位置に集積された能動素子及び前記半導体基板の他の位置に集積され、前記半導体基板に選択的に形成された垂直溝と、この垂直溝の内壁面に形成された絶縁膜と、前記垂直溝内に絶縁膜を介在して埋設され、前記半導体基板の垂直方向に抵抗幅を有すると共に前記半導体基板の水平方向に抵抗長を有し、不純物がドープされて所望の抵抗値を有するように形成された多結晶半導体からなる抵抗体とから構成された抵抗素子を含むことを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、抵抗素子に関し、特に、半導体装置の一構成素子として能動素子と同一半導体基板に集積される抵抗素子に適用して有効な技術に関するものである。

【0002】

【従来の技術】ＩＣ、ＬＳＩ等の半導体装置は、能動素子として動作するトランジスタ以外に受動素子として動作する抵抗素子が同一半導体基板に集積される。この抵抗素子は半導体基板にトランジスタを製造する場合の製造工程の一部の工程を利用して、同時に同一半導体基板に製造される。例えばトランジスタの製造工程である拡散工程の一部を利用して、抵抗素子はトランジスタと同一半導体基板に製造される。

【0003】このような抵抗素子の製造については、オーム社発行「半導体集積回路入門」、昭和４２年５月２５日第１版発行、Ｐ１０２～Ｐ１０３に記載されている。この文献には、拡散によって製造する抵抗は、トランジスタのエミッタ層の拡散と同時か、あるいはベース層の拡散と同時に行なわれることが開示されている。このようにして製造される抵抗素子の抵抗値は、半導体基板の表面と水平方向に共に設定される抵抗長Ｌ及び抵抗幅Ｗの値に依存して決定される。すなわち、半導体基板

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の水平方向に抵抗長Ｌ及び抵抗幅Ｗを設定することにより、各値に依存した必要な抵抗値を得るようになっている。

【0004】

【発明が解決しようとする課題】前記抵抗素子を半導体基板に製造する場合、所望の抵抗値を得るにはこの抵抗値に応じて半導体基板の水平方向に抵抗長Ｌ及び抵抗幅Ｗを設定しなければならないので、抵抗値によっては抵抗長Ｌ及び抵抗幅Ｗの水平方向の値が大きくなるのは避けられない。従って、半導体基板に占めるレイアウト面積が大きくなるという問題が生ずる。

【0005】また、この抵抗素子をトランジスタのような能動素子と同一半導体基板に集積して半導体装置を製造する場合、半導体装置の集積度の向上を図るにはトランジスタのレイアウト面積だけでなく抵抗素子のレイアウト面積も縮小することが不可欠となる。ここで、トランジスタのレイアウト面積は最近のプロセス加工技術の向上により縮小が比較的容易であるが、抵抗素子に関しては前記のような理由によって、レイアウト面積の縮小は困難となる。また、無理に抵抗素子のレイアウト面積を縮小しようとすると、抵抗素子はもともと製造において抵抗値が大きくばらつき易いので、縮小に伴って半導体装置の特性変動に影響を及ぼすようになる。

【0006】本発明の目的は、レイアウト面積の縮小が容易な抵抗素子を提供することにある。

【0007】本発明の他の目的は、抵抗値のばらつきを小さく抑えたままレイアウト面積の縮小が容易な抵抗素子を提供することにある。

【0008】本発明のその他の目的は、抵抗値のばらつきを小さく抑えたまま抵抗素子のレイアウト面積の縮小を容易にすることにより、半導体装置の特性変動に及ぼす影響を最低限に抑えて、集積度の向上を図る半導体装置を提供することにある。

【0009】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【0010】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば下記の通りである。

【0011】（1）本発明の抵抗素子は、基板に選択的に垂直溝が形成され、この基板の垂直溝の内壁面には絶縁膜が形成されている。基板の垂直溝内には絶縁膜を介在して基板の垂直方向に抵抗幅を有すると共に、基板の水平方向に抵抗長を有する抵抗体が埋設されている。

【0012】（2）本発明の他の抵抗素子は、半導体基板に選択的に垂直溝が形成され、この半導体基板の垂直溝の内壁面には絶縁膜が形成されている。半導体基板の垂直溝内には絶縁膜を介在して、半導体基板の垂直方向に抵抗幅を有すると共に半導体基板の水平方向に抵抗長

を有し、不純物がドープされて所望の抵抗値を有するように形成された多結晶半導体からなる抵抗体が埋設されている。

【0013】（3）本発明の半導体装置は、半導体基板の所望の位置には能動素子が集積されている。また、半導体基板の他の位置には、この半導体基板に選択的に形成された垂直溝と、この垂直溝の内壁面に形成された絶縁膜と、前記垂直溝内に絶縁膜を介在して埋設され、前記半導体基板の垂直方向に抵抗幅を有すると共に前記半導体基板の水平方向に抵抗長を有し、不純物がドープされて所望の抵抗値を有するように形成された多結晶半導体からなる抵抗体とから構成された抵抗素子が集積されている。

【0014】

【作用】上述した（1）の手段によれば、本発明の抵抗素子は、基板の垂直溝内に絶縁膜を介在して基板の垂直方向に抵抗幅を有すると共に、基板の水平方向に抵抗長を有する抵抗体が埋設されて構成されるので、抵抗素子のレイアウト面積の縮小が容易になる。

【0015】上述した（2）の手段によれば、本発明の抵抗素子は、半導体基板の垂直溝内に絶縁膜を介在して半導体基板の垂直方向に抵抗幅を有すると共に半導体基板の水平方向に抵抗長を有し、不純物がドープされて所望の抵抗値を有する多結晶半導体からなる抵抗体が埋設されて構成されるので、抵抗値のばらつきを小さく抑えたまま抵抗素子のレイアウト面積の縮小が容易になる。

【0016】上述した（3）の手段によれば、本発明の半導体装置は、同一半導体基板の所望の位置に能動素子が集積され、他の位置には、前記半導体基板の垂直溝内に絶縁膜を介在して半導体基板の垂直方向に抵抗幅を有すると共に半導体基板の水平方向に抵抗長を有し、不純物がドープされて所望の抵抗値を有する多結晶半導体からなる抵抗体が埋設されて構成された抵抗素子が集積されるので、抵抗値のばらつきを小さく抑えたまま抵抗素子のレイアウト面積の縮小が容易になり、半導体装置の特性変動に及ぼす影響を最低限に抑えて、集積度の向上を図ることができる。

【0017】

【実施例】以下図面を参照して本発明の実施例を説明する。

【0018】（実施例1）図1は本発明の実施例1による抵抗素子を示す斜視図で、図2は図1のA－A断面図である。1は例えばP導電型のシリコン単結晶基板からなる基板で、この基板1には選択的に垂直溝2が形成されている。この垂直溝2は、いわゆるトレンチ構造を有しており、基板1の水平方向hの寸法d（後述の厚さdに相当）よりも大きい垂直方向Vの寸法W（後述の抵抗幅Wに相当）を有すると共に、その水平方向hと直交する他の水平方向Hの寸法L（後述の抵抗長Lに相当）を有している。なお、水平方向h及びこれと直交する他の水平方向Hは相対的な関係を示しており、基板1の表面に水平方向であればいずれもどのような向きにも選ぶことができる。このような垂直溝2は異方性エッチング処理等の加工技術を用いて形成される。例えば、この垂直溝2は、後述するように、リアクティブ・イオン・エッチング（Ｒｅａｃｔｉｖｅ　Ｉｏｎ　Ｅｔｃｈｉｎｇ）による異方性エッチングによって形成される。

【0019】3は例えば二酸化シリコン（ＳｉO2）からなる絶縁膜で、ＣＶＤ法等の気相成長技術を用いて、垂直溝2の内壁面に形成される。4は例えば多結晶シリコンからなる抵抗体で、ＣＶＤ法等の気相成長技術を用いて形成されて、垂直溝2内に絶縁膜3を介在して埋設される。この多結晶シリコンからなる抵抗体4には不純物例えばボロン、燐、砒素、アンチモン等がイオン打ち込み法等を用いてドープされて、所望の抵抗値を有するように形成されている。ここで、この多結晶シリコンからなる抵抗体4は基板1の垂直方向Vに抵抗幅Wを有するとともに、基板1の水平方向Hに抵抗長Lを有するように形成され、さらに水平方向hに厚さdを有するように形成されている。

【0020】これにより、この抵抗体4は、（抵抗幅W×抵抗長L×厚さd）で決定される所望の抵抗値を有することになる。ここで、（抵抗幅W×厚さd）＝Aの値は抵抗体4の断面積を示しており、抵抗値は（断面積A×抵抗長L）で示されるので、一定の抵抗値を得る場合には、抵抗幅Wを大きく設定することにより、抵抗長Lは小さくできることになる。このことは、基板1に占める抵抗体4のレイアウト面積が小さくできることを意味している。

【0021】図2に示すように、所望の抵抗値を有するように形成された多結晶シリコンからなる抵抗体4には、基板1の絶縁膜3上に例えばアルミニウムからなる一対の電極5が引き出されることによって、抵抗素子7として構成される。抵抗体4の表面は二酸化シリコン等の絶縁膜6によって保護される。基板1の抵抗素子7が形成された位置以外の表面は絶縁膜3あるいは他の絶縁膜によって保護される。

【0022】次に、図3乃至図7を参照して実施例1の抵抗素子の製造方法を工程順に説明する。図3に示すように、まず、P導電型のシリコン単結晶基板からなる基板1を用意して、この基板1の垂直溝を形成すべき表面以外にフォトレジスト8を塗布する。次に、図4に示すように、基板1に対して例えばＳF6 とＣＣ14 との混合ガスを供給して、ＲＩＥによる異法性エッチングを行って、フォトレジスト8が塗布されていない基板1表面に選択的に、前記のように垂直方向Vに寸法W、水平方向hに寸法d、他の水平方向Hに寸法Lを有する垂直溝2を形成する。続いて、フォトレジスト8を除去した後、図5に示すように、基板1に対して例えばＳｉH4 とO2 との混合ガスを供給して、ＣＶＤによる気相成長

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を行って、垂直溝２の内壁面を含む基板１表面に二酸化シリコンからなる絶縁膜３を形成する。

【００２３】次に、図６に示すように、基板１に対して例えばＳｉＣｌ4 とH2 との混合ガスを供給して、ＣＶＤによる気相成長を行って、垂直溝２内に絶縁膜３を介在して多結晶シリコンからなる抵抗体４を埋設する。続いて、図７に示すように、この多結晶シリコンからなる抵抗体４に例えば＋ボロンイオンをイオン打ち込み法により打ち込んだ後、熱処理を施すことにより、ボロンをドープして抵抗体４を所望の抵抗値に制御する。ボロンの打ち込みに際しては、不要部分をフォトレジスト８でマスクしておくことにより、多結晶シリコンからなる抵抗体４に対してのみボロンをドープすることができる。

【００２４】次に、図２に示すように、多結晶シリコンからなる抵抗体４の両端部から基板１の絶縁膜３上に一対の電極５を引き出すように形成する。これは、例えばアルミニウムをＣＶＤ法等により全面に付着したのち、フォトエッチングを行って、不要部分を除去することにより行う。続いて、抵抗体４の表面に例えば二酸化シリコンからなる絶縁膜６を、前記のようなＣＶＤ法等を用いて形成する。基板１の表面の絶縁膜３は図５の工程時に形成された二酸化シリコンをそのまま用いても良く、あるいは基板１から熱的に成長した二酸化シリコンを用いても良い。以上の各工程によって実施例１の抵抗素子７が製造される。

【００２５】このような実施例１によれば次のような効果が得られる。

【００２６】（１）抵抗素子７は、基板１の垂直溝２内に絶縁膜３を介在して基板１の垂直方向Ｖに抵抗幅Ｗを有すると共に、基板１の水平方向Ｈに抵抗長Ｌを有する抵抗体４が埋設されて構成されるので、抵抗幅Ｗを垂直方向Ｖに大きくとることにより水平方向Ｈの抵抗長Ｌは小さくして所望の抵抗値が得られるため、抵抗素子７のレイアウト面積の縮小が容易になる。

【００２７】（２）抵抗素子７は、半導体基板からなる基板１の垂直溝２内に絶縁膜３を介在して基板１の垂直方向Ｖに抵抗幅Ｗを有すると共に基板１の水平方向Ｈに抵抗長Ｌを有し、不純物がドープされて所望の抵抗値を有する多結晶半導体からなる抵抗体４が埋設されて構成されるので、不純物のドープ量により所望の抵抗値が得られるため、抵抗値のばらつきを小さく抑えたま抵抗素子７のレイアウト面積の縮小が容易になる。

【００２８】（実施例２）図９は実施例２による半導体装置を示す断面図で、図８に示したような回路構成の例えばＮＰＮトランジスタからなるトランジスタ１０及びこのトランジスタ１０のエミッタ領域に接続する抵抗素子７を同一半導体基板に集積した構造を示すもので、図１０は図９の配線パターンを示す上面図である。半導体装置１６の例えばＰ導電型のシリコン単結晶基板からなる基板１の所望位置であるアイソレーション領域９で絶

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縁されたアイランド１１には、Ｎ導電型のコレクタ領域１２、このコレクタ領域１２内に選択的に形成されたＰ導電型のベース領域１３、このベース領域１３内に選択的に形成されたＮ導電型のエミッタ領域１４からなる能動素子として動作するＮＰＮ型トランジスタからなるトランジスタ１０が集積されている。コレクタ領域１２、ベース領域１３、エミッタ領域１４は拡散法、イオン打ち込み法等を用いて形成される。トランジスタ１０の表面は各領域１２、１３、１４の形成時成長した例えば二酸化シリコンからなる絶縁膜１５で保護されている。なお、各領域１２、１３、１４の導電型は一例を示したものであり、逆の導電型を選ぶことができる。

【００２９】一方、半導体装置１６の基板１の他の位置には、基板１に選択的に形成された垂直方向Ｖに寸法Ｗ、水平方向ｈに寸法ｄ、他の水平方向Ｈに寸法Ｌを有する垂直溝２と、この垂直溝２の内壁面に形成された例えば二酸化シリコンからなる絶縁膜３と、垂直溝２内に絶縁膜３を介在して埋設され、基板１の垂直方向Ｖに抵抗幅Ｗを有すると共に基板１の水平方向Ｈに抵抗長Ｌを有し、不純物がドープされて所望の抵抗値を有するように形成された多結晶半導体からなる抵抗体４とから構成され、この抵抗体４から引き出された例えばアルミニウムからなる一対の電極５を有する抵抗素子７が集積されている。この抵抗素子７は前記の製造方法によって製造される。

【００３０】抵抗素子７から引き出された一対の電極５の一方は、絶縁膜１５上を延長されて、トランジスタ１０のエミッタ領域１４上の絶縁膜１５に形成されたコンタクトホール１４Ｅを通してエミッタ領域１４に接続されて、エミッタ電極１４ｅとして働く。また、ベース領域１３上の絶縁膜１５に形成されたコンタクトホール１３Ｂを通してベース電極１３ｂが引き出されており、さらに、コレクタ１２上の絶縁膜１５に形成されたコンタクトホール１２Ｃを通してコレクタ電極１２ｃが引き出されている。

【００３１】このような実施例２によれば次のような効果が得られる。

【００３２】半導体装置１６は、同一基板１の所望の位置に能動素子として動作するトランジスタ１０が集積され、他の位置には、前記実施例１で示された構造の抵抗素子７が集積されるので、抵抗値のばらつきを小さく抑えたまま抵抗素子７のレイアウト面積の縮小が容易になり、半導体装置１６の特性変動に及ぼす影響を最低限に抑えて、集積度の向上を図ることができる。

【００３３】以上、本発明者によってなされた発明を、前記実施例に基づき具体的に説明したが、本発明は、前記実施例に限定されるものではなく、その要旨を逸脱しない範囲において種々変更可能であることは勿論である。

【００３４】例えば、前記各実施例では基板１としては

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シリコン単結晶基板を用いる例で説明したが、この基板1はシリコンに限らず他の半導体材料からなる単結晶基板を用いることができる。また、この基板1は半導体材料に限らず、例えばセラミックスのような絶縁材料からなるものを用いるようにしても良い。このように絶縁材料からなる基板1を用いた場合には、半導体装置を構成する能動素子として動作するトランジスタはチップの形でこの基板1の表面に実装される。

【0035】また、前記各実施例では絶縁膜3としては二酸化シリコンを用いる例で説明したが、この絶縁膜3はこれに限らず他の絶縁材料を用いることができる。例えば窒化シリコン（Si3N4）、酸化アルミニウム（Al2O3）等の他の絶縁材料を用いることができ、これらの絶縁材料は二酸化シリコンの場合と同様にCVD法等の気相成長技術を用いて形成することができる。さらに、この絶縁膜3は一層に限らず同一材料あるいは異なる材料からなる複数層から形成されていても良い。

【0036】また、前記実施例では抵抗体4としては多結晶シリコンを用いる例で説明したが、この抵抗体4はシリコンに限らず他の半導体材料を用いることができる。さらに、この抵抗体4にドープする不純物はボロンのような特定の不純物に限ることなく、燐、砒素、アンチモン等のその他の不純物を用いることができる。さらにまた、この抵抗体4としては半導体材料以外の抵抗材料を用いるようにしても良い。

【0037】以上の説明では主として本発明者によってなされた発明をその背景となった利用分野である抵抗素子の形成技術に適用した場合について説明したが、それに限定されるものではない。本発明は、少なくとも基板に垂直溝を形成して、この垂直溝内に抵抗体を埋設して素子を形成する条件のものには適用できる。

【0038】

【発明の効果】本願において開示される発明のうち代表的なものによって得られる効果を簡単に説明すれば、下記の通りである。

【0039】抵抗素子のレイアウト面積の縮小が容易になる。

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【0040】抵抗値のばらつきを小さく抑えたまま抵抗素子のレイアウト面積の縮小が容易になる。

【0041】抵抗値のばらつきを小さく抑えたまま抵抗素子のレイアウト面積の縮小が容易になり、半導体装置の特性変動に及ぼす影響を最低限に抑えて、集積度の向上を図ることができる。

【図面の簡単な説明】

【図1】本発明の実施例1による抵抗素子を示す斜視図である。

【図2】図1のA－A断面図である。

【図3】本発明の実施例1による抵抗素子の製造方法の一工程を示す断面図である。

【図4】本発明の実施例1による抵抗素子の製造方法の他の工程を示す断面図である。

【図5】本発明の実施例1による抵抗素子の製造方法のその他の工程を示す断面図である。

【図6】本発明の実施例1による抵抗素子の製造方法のその他の工程を示す断面図である。

【図7】本発明の実施例1による抵抗素子の製造方法のその他の工程を示す断面図である。

【図8】本発明の実施例2による半導体装置の回路構成図である。

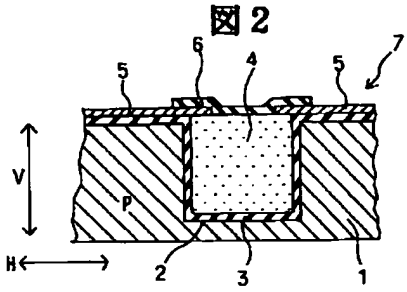
【図9】本発明の実施例2による半導体装置を示す断面図である。

【図10】本発明の実施例2による半導体装置を示す上面図である。

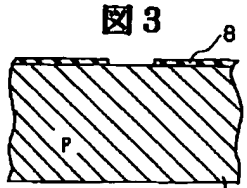
【符号の説明】

1…基板、2…垂直溝、3…絶縁膜、4…抵抗体、5…一対の電極、6…絶縁膜、7…抵抗素子、8…フォトレジスト、9…アイソレーション領域、10…トランジスタ（能動素子）、11…アイランド、12…コレクタ領域、12E…コレクタコンタクトホール、12e…コレクタ電極、13…ベース領域、13B…ベースコンタクトホール、13b…ベース電極、14…エミッタ領域、14E…エミッタコンタクトホール、14e…エミッタ電極、15…絶縁膜、16…半導体装置。

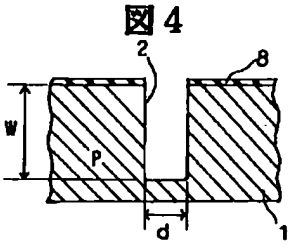
【図2】



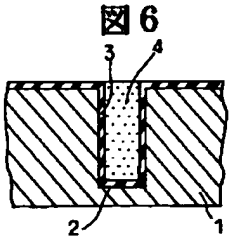
【図3】



【図4】

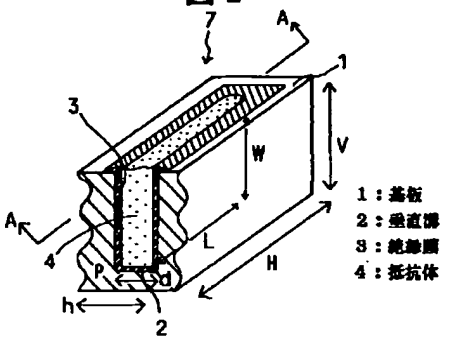


【図6】



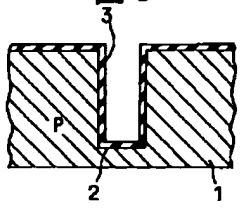
【図1】

図1



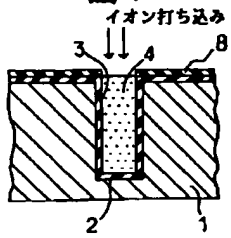
【図5】

図5



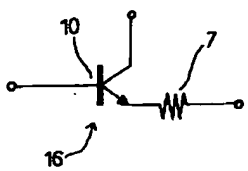
【図7】

図7



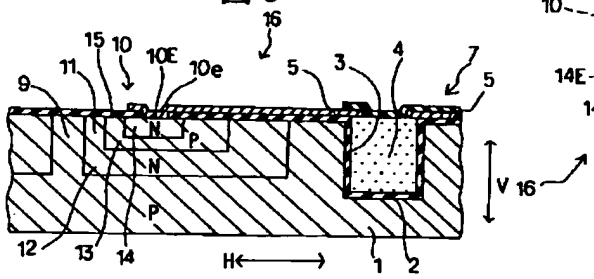
【図8】

図8



【図9】

図9



【図10】

図10